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**Industrial microSD Memory Cards
Engineering Specification**

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| Revision | Change Description | Date |
|----------|---------------------|-----------|
| A | Preliminary Release | 3/21/2008 |
| | | |



General Description

The microSD is currently the world's smallest removable storage card (roughly a quarter of the size of the standard SD card) and is the newest standard of SD flash memory. This card is specifically designed for use in small devices such as mobile phones and GPS systems, and is fully compatible with current SD devices when used with the included adapter. Like the miniSD, the microSD is ideal for storing media-rich files such as music, videos, and photographs. The card is supported in approximately 30 percent of handsets announced by manufacturers such as Motorola, Samsung, LG, Kyocera, and Sagem, as well as many GPS systems on the market.

Applications

- Industrial Computer
- Embedded Systems
- Data Acquisition
- Automotive
- Flight Systems
- Also, hundreds of other industries looking for a more robust and rugged digital storage option
- Agriculture
- Manufacturing
- Military
- Gaming
- Telecommunications

Features

- Compliant with SD Spec. – Version 1.10 and SDHC Spec. – Version 2.0
- Operating bus modes – SD & SPI
- SD capacities supported: up to 2 GB
- SDHC capacities supported: up to 32GB
- Solid State Memory
- Supports 2.7Volt to 3.6Volt operation

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1.0 General microSD Card Specifications

1.1 Recommended Temperature Conditions

| <u>Parameter</u> | <u>Min.</u> | <u>Max.</u> |
|----------------------------|-------------|-------------|
| Storage Temp. | -40°C | 85°C |
| Industrial Operating Temp. | -10°C | 85°C |

1.2 Performance

| <u>Parameter</u> | <u>Value</u> |
|---------------------------|-----------------------|
| *Data Transfer Rate Read | up to 23 MB/sec (Max) |
| *Data Transfer Rate Write | up to 20 MB/sec (Max) |

* Dependant on configuration and testing environment

1.3 Card Dimensions

Table 1 - microSD Card Dimensions

| | |
|--|-----------------------------------|
| Length: | 15 ± 0.10 mm (0.59 ± .004 in.) |
| Width: | 11 ± 0.10 mm (0.43 ± .004 in.) |
| Thickness Including Label Area: | 1 mm ± 0.15 mm (0.039 ± .006 in.) |

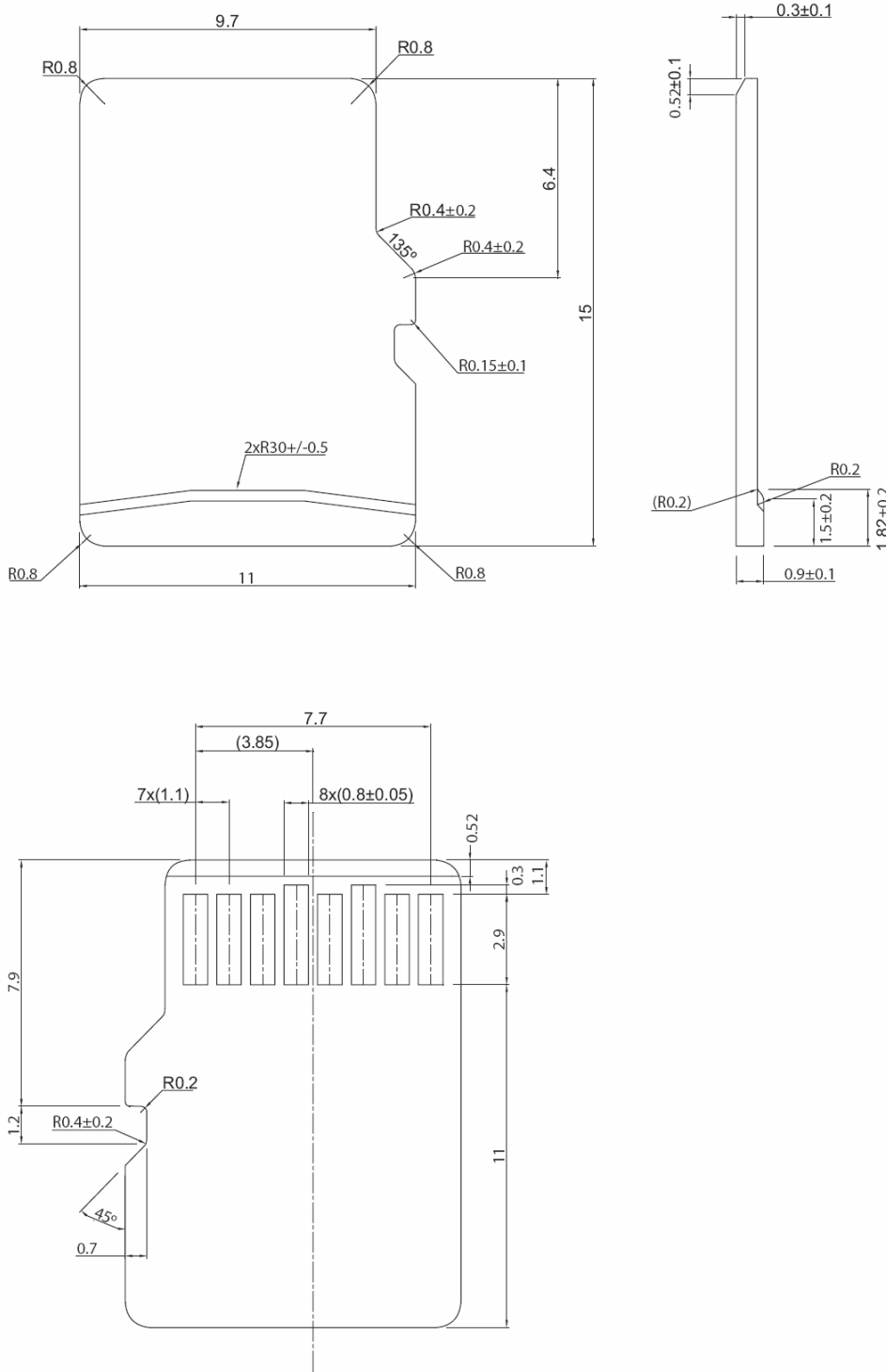


Fig 1 - microSD Card Dimensions

2.0 microSD Card Interface

2.1 microSD Pin Assignment

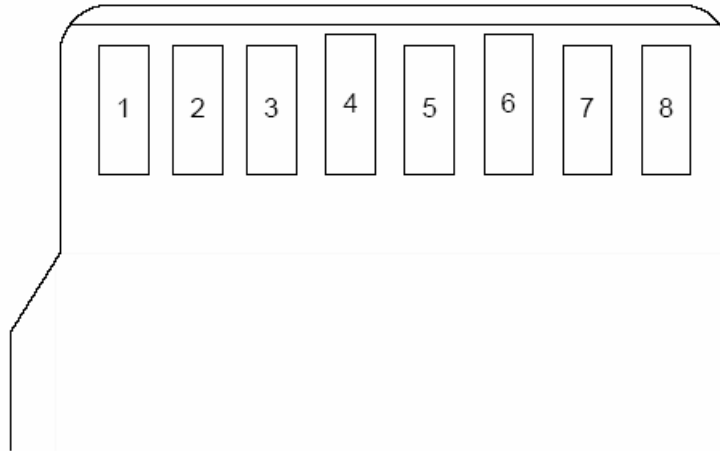


Fig 2 - microSD Card Pin Designation

Table 2 - microSD SD BUS Mode Pin Assignment

| Pins | Symbol | Type | Description |
|------|---------|--------------|-------------------------|
| 1 | DAT2 | Input/Output | Data Line: Bit 2 |
| 2 | CD/DAT3 | Input/Output | Card Detect/Data Line 3 |
| 3 | CMD | Input/Output | Command/Response |
| 4 | VDD | Supply | Power Supply |
| 5 | CLK | Input | Clock |
| 6 | Vss | Supply | Ground |
| 7 | DAT0 | Input/Output | Data Line: Bit 0 |
| 8 | DAT1 | Input/Output | Data Line: Bit 1 |

Table 3 - microSD SPI BUS Mode Pin Assignment

| Pins | Symbol | Type | Description |
|------|--------|--------|------------------------|
| 1 | RSV | | Reserved |
| 2 | CS | Input | Chip Select (neg true) |
| 3 | DI | Supply | Data In |
| 4 | VDD | Supply | Supply Voltage |
| 5 | SCLK | Input | Clock |
| 6 | Vss | Supply | Supply Voltage Ground |
| 7 | DO | Output | Data Out |
| 8 | RSV | Input | Reserved |

2.2 SD Bus Topology

The microSD Memory Card supports two alternative communication protocols: SD and SPI Bus Mode. Host System can choose either one of modes. The same Data of the microSD Card can be read and written in both modes. SD Mode allows the 4-bit high performance data transfer. SPI Mode allows easy and common interface for SPI channel. The disadvantage SPI mode is loss of performance, relatively to the SD mode.

2.3 SD Bus Mode protocol

The microSD uses the SD bus mode. The SD bus allows the dynamic configuration of the number of data line from 1 to 4 Bi-directional data signal. After power up by default, the SD card will use only DAT0. After initialization, host can change the bus width.

Multiplied SD cards connections are available to the host. Common Vdd, Vss and CLK signal connections are available in the multiple connections. However, Command, Respond and Data lined (DAT0-DAT3) shall be divided for each card from host. This feature allows easy trade off between hardware cost and system performance. Communication over the SD bus is based on command and data bit stream initiated by a start bit and terminated by stop bit.

Command:

Commands are transferred serially on the CMD line. A command is a token to starts an operation from host to the card. Commands are sent to an addressed single card (addressed Command) or to all connected cards (Broad cast command).

Response:

Responses are transferred serially on the CMD line. A response is a token to answer to a previous received command. Responses are sent from an addressed single card or from all connected cards.

Data:

Data can be transfer from the card to the host or vice versa. Data is transferred via the data lines.

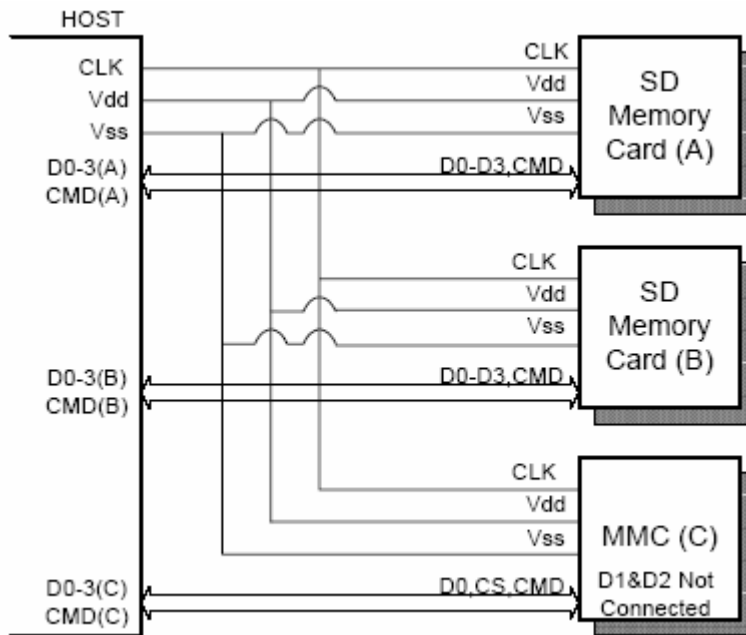


Fig 3 - microSD Card (SD Mode) Connection Diagram

- CLK: Host card Clock signal
- CMD: Bi-directional Command/ Response Signal
- DAT0 - DAT3: 4 Bi-directional data signal
- V_{dd}: Power supply
- V_{ss}: GND

For more information on the SD Mode Command Set [*SD Spec. – Part 1 Physical Layer Specification Version 1.10*](#).

2.4 SPI Bus Mode Protocol

The SPI bus allows 1 bit Data line by 2-chanel (Data In and Out). The SPI compatible mode allows the MMC Host systems to use SD card with little change. The SPI bus mode protocol is byte transfers. All of the data token are multiples of the bytes (8-bit) and always byte aligned to the CS signal.

The advantage of the SPI mode is reducing the host design in effort. Especially, MMC host can be modified with little change. The disadvantage of the SPI mode is the loss of performance versus SD mode. Caution: Please use SD Card Specification. DO NOT use MMC Specification. For example, initialization is achieved by ACMD41, and be careful to Register. Register definition is different, especially CSD Register.

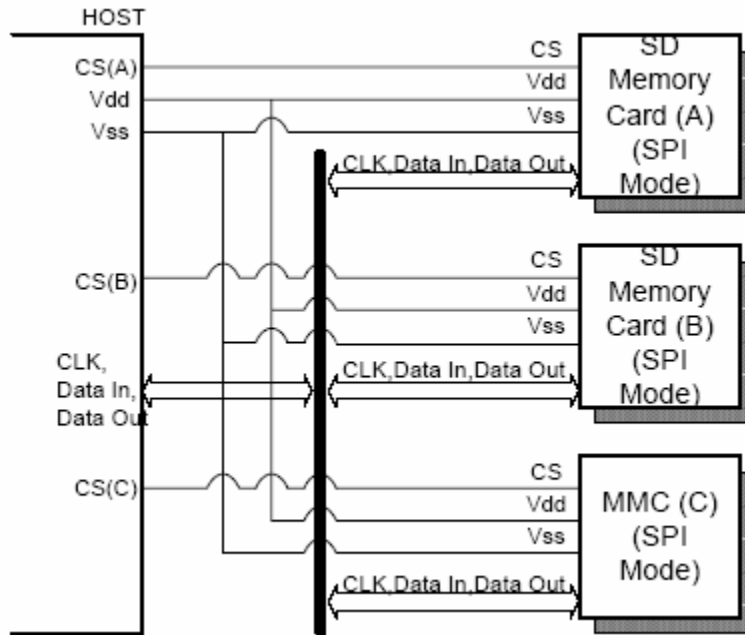


Fig 4 - SD Card (SPI Mode) Connection Diagram

- CS: Card Select Signal
- CLK: Host card Clock signal
- Data in: Host to card data line
- Data out: card to host data line
- V_{dd}: Power supply
- V_{ss}: GND

For more information on the SPI Mode Command Set refer to [SD Spec. – Part 1 Physical Layer Specification Version 1.10](#).

3.0 microSD Card Electrical Characteristics

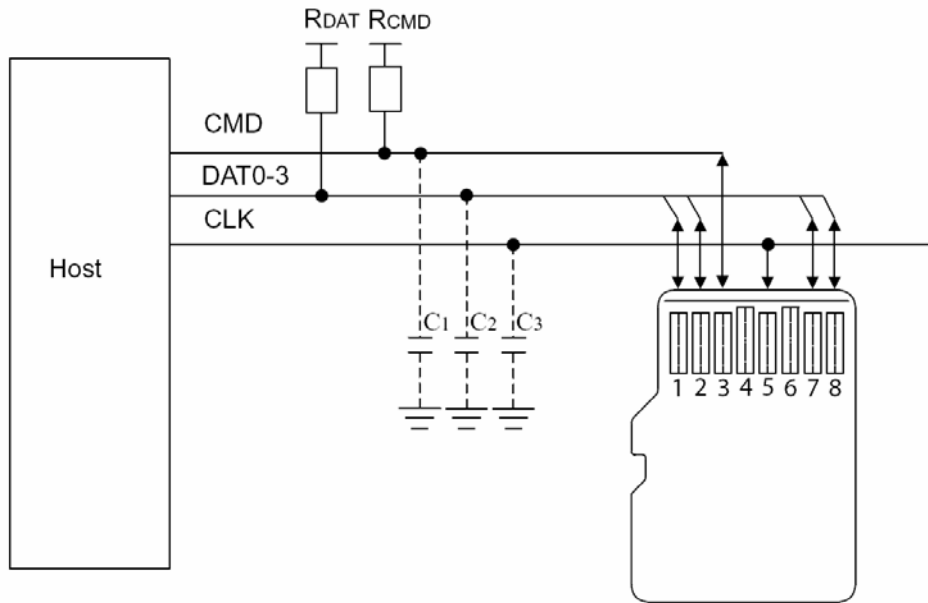


Fig 5 - microSD Card Connection Diagram

3.1 Absolute Maximum Conditions

Table 4 - Absolute Maximum Conditions

| Item | Symbol | Value | Unit |
|----------------|-------------------|----------------------------------|------|
| Supply Voltage | $V_{DD} - V_{SS}$ | -0.3 to 3.3 | V |
| Input Voltage | V_{IN} | $V_{SS} - 0.3$ to $V_{DD} + 0.3$ | V |

3.2 DC Characteristics

Table 5 - DC Characteristics

| Parameter | Symbol | Min | Max | Unit | Notes |
|---------------------|----------|------------------|------------------|------|--|
| Input LOW Voltage | V_{IL} | $V_{SS} - 0.3$ | $0.25 * V_{DD}$ | V | |
| Input HIGH Voltage | V_{IH} | $0.625 * V_{DD}$ | $V_{DD} + 0.3$ | V | |
| Output LOW Voltage | V_{OL} | | $0.125 * V_{DD}$ | V | $I_{OH} = -100\mu A$ @ V_{DD} Min |
| Output HIGH Voltage | V_{OH} | $0.75 * V_{DD}$ | | V | $I_{OL} = 100\mu A$ @ V_{DD} Min |

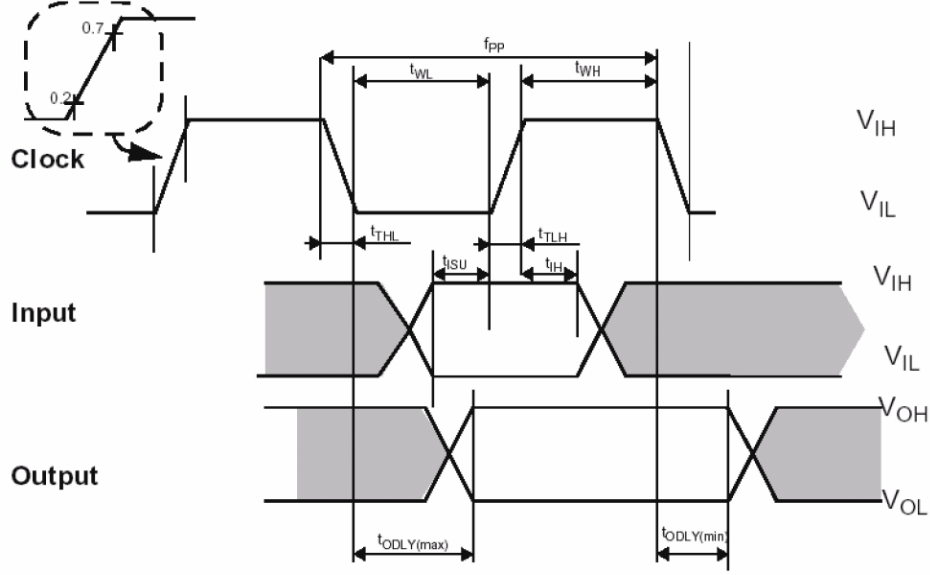
Table 6 - Signal Capacitance

| Item | Symbol | Min. | Max. | Unit | Notes |
|--------------------------------------|------------------------|------|------|----------|----------------------------------|
| Pull up Resistance | R_{CMD} R_{DAT} | 10 | 100 | K Ohm | |
| Bus Signal Line Capacitance | C_L | - | 250 | pF | $F_{PP} < 5\text{MHz}$ (21Cards) |
| Bus Signal Line Capacitance | C_L | - | 100 | pF | $F_{PP} < 20\text{MHz}$ (7Cards) |
| Single Card Capacitance | C_{CARD} | - | 10 | pF | |
| Pull up Resistance inside card(pin1) | R_{DAT3} | 10 | 90 | K Ohm | |

Note: WP pull-up (R_{wp}) Value is dependant on the Host Interface drive circuit.

3.3 AC Characteristics

3.3.1 SD Interface timing



Shaded areas are not valid

Fig 6 - AC Timing Diagram

Table 7 - AC Characteristics

| Parameter | Symbol | Min. | Max. | Unit | Notes |
|---|------------|------|------|------|--------------------------------|
| Clock CLK (All values are referred to min(V_{IH}) and max(V_{IL})) | | | | | |
| Clock frequency Data Transfer Mode | f_{pp} | 0 | 25 | MHz | $CL \leq 100$ pF (7cards) |
| Clock frequency Identification Mode (the low freq. is required for MultiMedia Card compatibility) | f_{OD} | 0 | 400 | KHz | $CL \leq 250$ pF (21 cards) |
| Clock low time | t_{WL} | 10 | | ns | $CL \leq 100$ pF (7cards) |
| Clock high time | t_{WH} | 10 | | ns | $CL \leq 100$ pF (7cards) |
| Clock rise time | t_{TLH} | | 10 | ns | $CL \leq 100$ pF (7cards) |
| Clock fall time | t_{THL} | | 10 | ns | $CL \leq 100$ pF (7cards) |
| Clock low time | t_{WL} | 50 | | ns | $CL \leq 250$ pF (21 cards) |
| Clock high time | t_{WH} | 50 | | ns | $CL \leq 250$ pF (21 cards) |
| Clock rise time | t_{TLH} | | 50 | ns | $CL \leq 250$ pF (21 cards) |
| Clock fall time | t_{THL} | | 50 | ns | $CL \leq 250$ pF (21 cards) |
| Inputs CMD, DAT (referenced to CLK) | | | | | |
| Input set-up time | t_{ISU} | 5 | | ns | $CL \leq 25$ pF (1 cards) |
| Input hold time | t_{IH} | 5 | | ns | $CL \leq 25$ pF (1 cards) |
| Outputs CMD, DAT (referenced to CLK) | | | | | |
| Output Delay time | t_{ODLY} | 0 | 14 | ns | $CL \leq 25$ pF (1 cards) |

Table 8 Flash Interface AC Characteristic

| Parameter | Symbol | Min | Max | Unit |
|--------------------|--------|-----|-----|------|
| CLE Set-up Time | tCLS | 50 | - | ns |
| CLE Hold Time | tCLH | 50 | - | ns |
| /CE Setup Time | tCS | 200 | - | ns |
| /CE Hold Time | tCH | 200 | - | ns |
| WE Pulse Width | tWP | 30 | 50 | ns |
| ALE Setup Time | tALS | 50 | - | ns |
| ALE Hold Time | tALH | 50 | - | ns |
| Data Setup Time | tDS | 20 | 50 | ns |
| Data Hold Time | tSH | 30 | 100 | ns |
| Write Cycle Time | tWC | 50 | 200 | ns |
| WE High Hold Time | tWH | 20 | 150 | ns |
| Read Cycle Time | tRC | 50 | - | ns |
| /RE Pulse Width | tRP | 30 | - | ns |
| /RE High Hold Time | tREH | 20 | - | ns |
| Ready to /RE Low | tRR | 30 | - | ns |

3.4 Flash Memory Timing

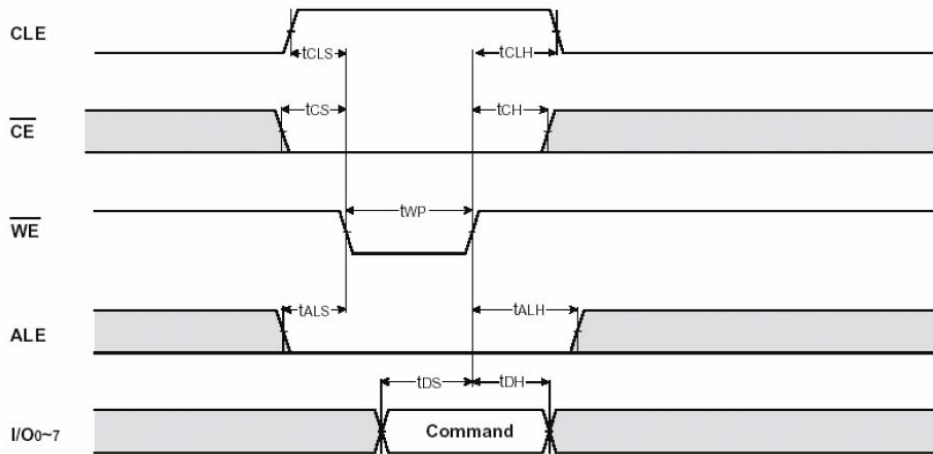


Fig 7 – Command Latch Cycle

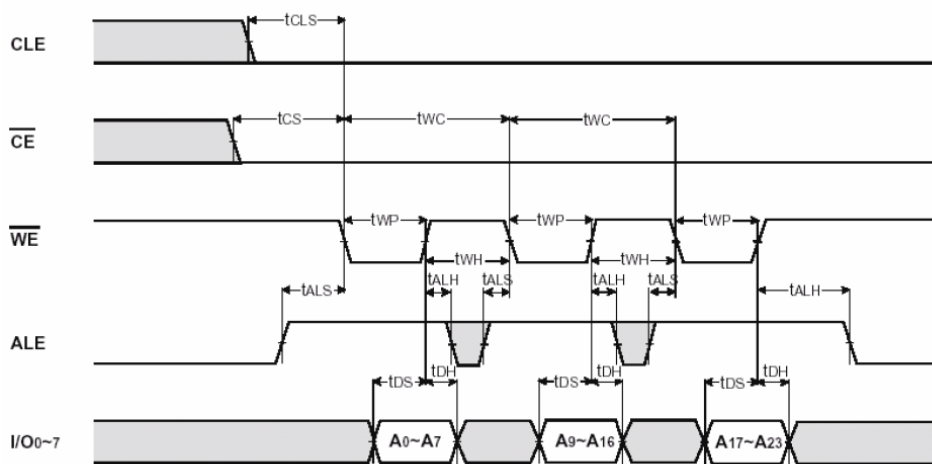


Fig 8 - Address Latch Cycle

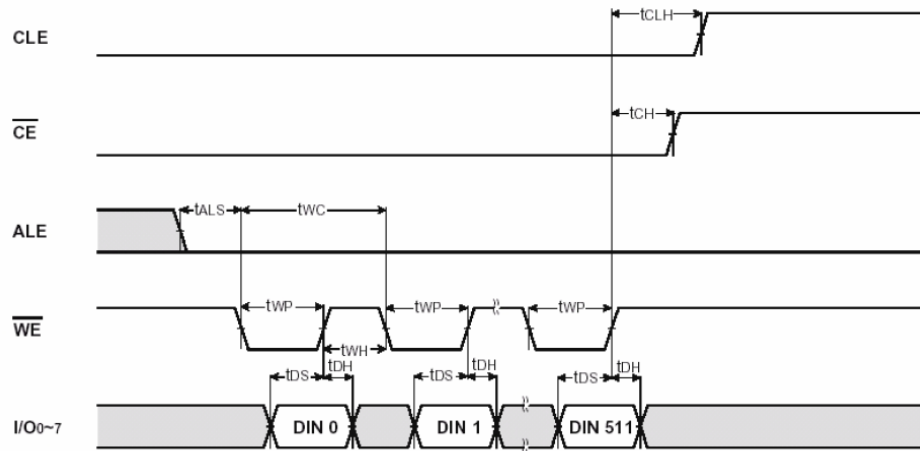


Fig 9 – Input Data Latch Cycle

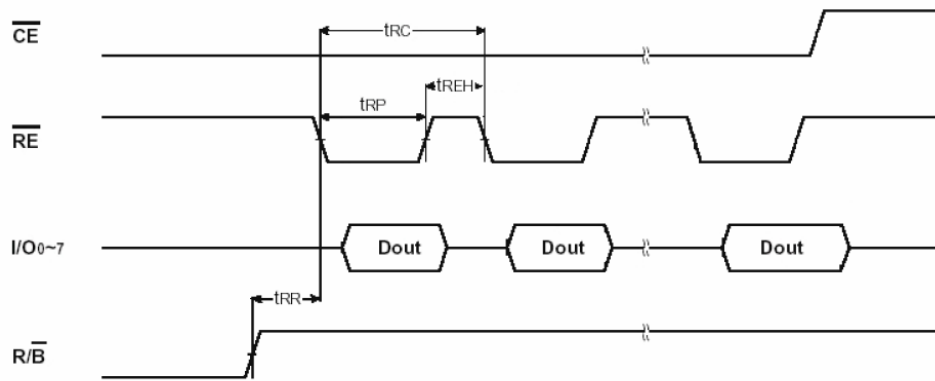


Fig 10 - Sequential Out Cycle after Read (CLE=L, /WE=H, ALE=L)